Patent
Attorney's Docket No. 015290-508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Paul K. Shufflebotham et al.	Group Art Unit: 1763
Application No.: 09/775,664	Examiner: Rudy Zervignon
Filed: February 5, 2001	Confirmation No.: 9320
For: INDUCTIVELY COUPLED PLASMA CVD	

DECLARATION BY BRIAN MCMILLIN AND BUTCH BERNEY UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Brian McMillin and Butch Berney, hereby state as follows:

1. We are two co-inventors of the subject matter claimed in U.S. Patent Application Serial No. 0/775,664, which is assigned to Lam Research Corporation ("Lam").

2. Exhibit A attached hereto is a copy of a sketch of an inductively coupled plasma CVD processing system. The CVD processing system includes a plasma processing chamber; a dielectric window forming a top wall of the plasma processing chamber; a substrate support adapted to support a substrate within the

processing chamber; and a plurality of injector tubes (two are shown in the plane of the sketch) adapted to introduce process gas into the processing chamber. As shown in Exhibit A, all of the injector tubes are spaced outwardly from the periphery of a substrate support on which a substrate is supported.

3. Exhibit B attached hereto is a copy of a sketch of approximately one-half of an inductively coupled plasma CVD processing system. The illustrated CVD processing system includes a plasma processing chamber; a dielectric window forming a top wall of the plasma processing chamber; a substrate support adapted to support a substrate within the processing chamber; and an injector tube adapted to introduce process gas into the processing chamber. The remaining approximately one-half of the CVD processing system that is not shown in Exhibit B also includes an injector tube in the plane of the sketch. As shown in Exhibit B, the injector tube is spaced outwardly from the periphery of a substrate supported on a substrate support.

4. The CVD processing system shown in Exhibits A and B was manufactured in the United States prior to June 28, 1996.

5. Prior to June 28, 1996, the CVD processing system shown in Exhibits A and B was tested at Lam's research facility in Fremont, California and shown to operate. As an example, the testing included performing CVD processing of wafers

using the following process conditions: SiH_4 flow rate of 60 sccm to 180 sccm/O_2 flow rate of 100 sccm to 270 sccm/TCP RF power of 500 watts to 1500 watts. SiO_2 deposition rates of from about 3000 Å/min to about 8000 Å/min were achieved under these process conditions.

6. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 9/28/04

Brian McMillin

Date: 9/28/04

Butch Berney

EXHIBIT A

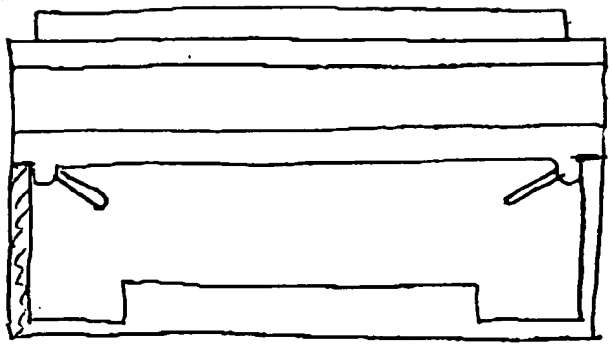

EXHIBIT B